SiGe Integrated Electronics for Extreme Environments

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Outline

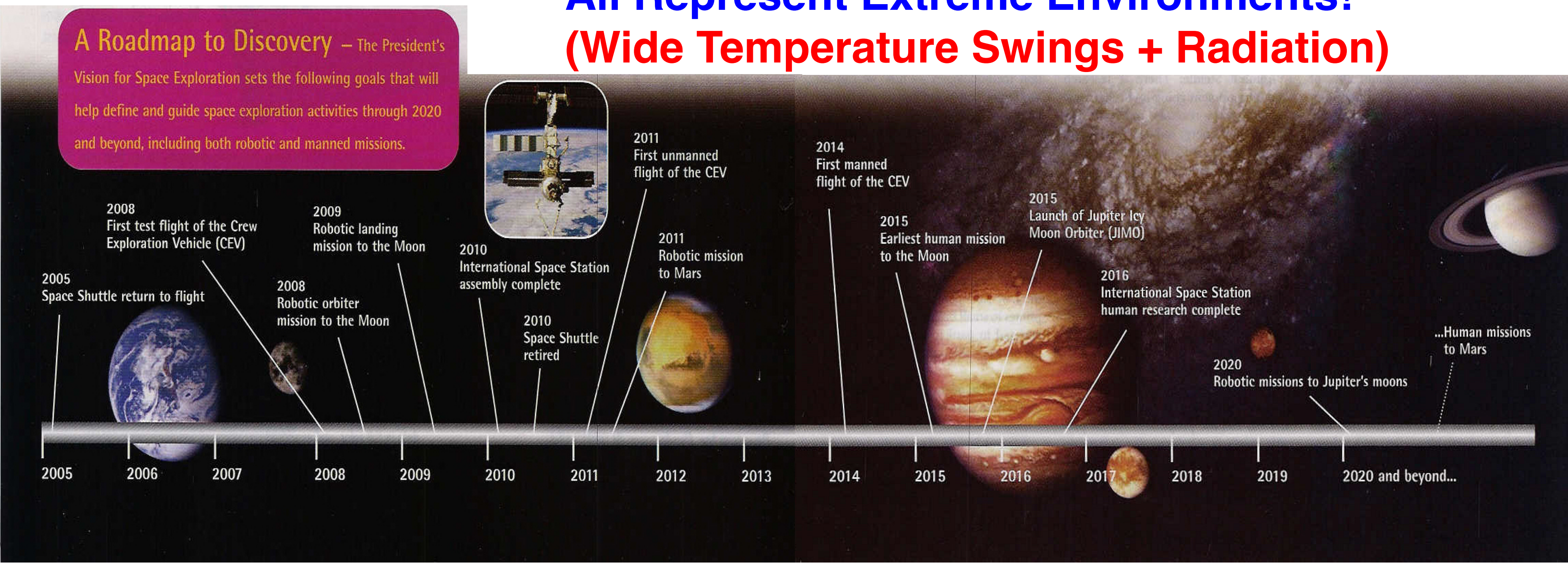
- Motivation
- SiGe Technology
- Phase I Project Highlights
- The Path Forward
- Summary

The Vision: Space Exploration

NASA ETDP: SiGe Integrated Electronics For Extreme Environments

All Represent Extreme Environments!

(Wide Temperature Swings + Radiation)



Moon **Mars** **Outer Planets**

Planet	$T_{surface}$ (K)	T_{sphere} (K)
Mercury	100-700	445
Venus	740	325
Earth	288-293	277
Mars	140-300	225
Jupiter	165	123
Saturn	134	90
Uranus	76	63
Neptune	72	50
Pluto	40	44

The Moon: A Classic Extreme Environment!

Temperature:

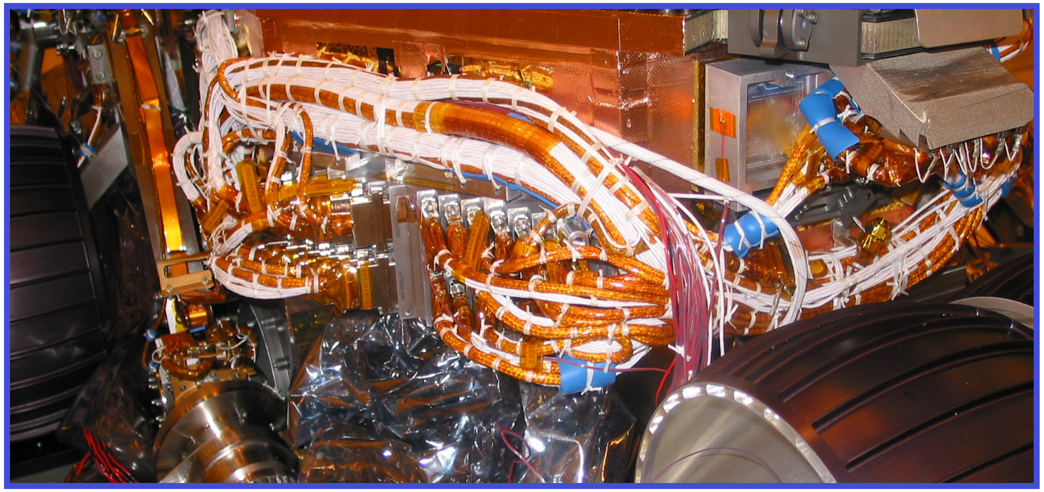
- +120C to -180C temperature swings
- 28 day cycles
- -230C in shadowed polar craters!

Radiation:

- 10's of krad (modest)
- (300 krad for Mars)
- single event upset
- solar events

Rover / Robotics

Current Practice: Centralized "Warm Box"



The Big Question…

Can We Design Mission-Critical Electronic Components That Reliably Operate at Ambient Conditions on the Moon / Mars?

WITH NO WARM BOX?!

Approach:

- Use SiGe BiCMOS (SiGe HBT + CMOS) as our IC Platform
- Plenty of Performance / Commercially Available
- Design Reliable Cryo-Packaging to Support the Circuits
- Develop the Requisite Infrastructure (reliability, models, etc.)
- Assemble a World Class Team To Pull It All Off!

Project Objectives

Objective:

Develop and Demonstrate Extreme Environment Electronic Components Required for Distributed Architecture Lunar / Martian Robotic / Vehicular Systems Using SiGe HBT BiCMOS Technology

Extreme Environments (e.g., Lunar):

- **+120C (day) to -180C (night) + cycling** (main focus)
- **radiation** (300 krad, SEU, and down to cryo-T)

- **Major Phase I Project Goals:**
  - prove SiGe BiCMOS technology for +120C to -180C applications
  - build and validate compact models for circuit design (design suite)
  - design and demonstrate mission-critical circuit component blocks (library)
  - develop and prove the packaging for these circuits
  - demonstrate device / package / circuit reliability per NASA specs
  - develop a robust maturation path for NASA mission insertion (TRL-6)

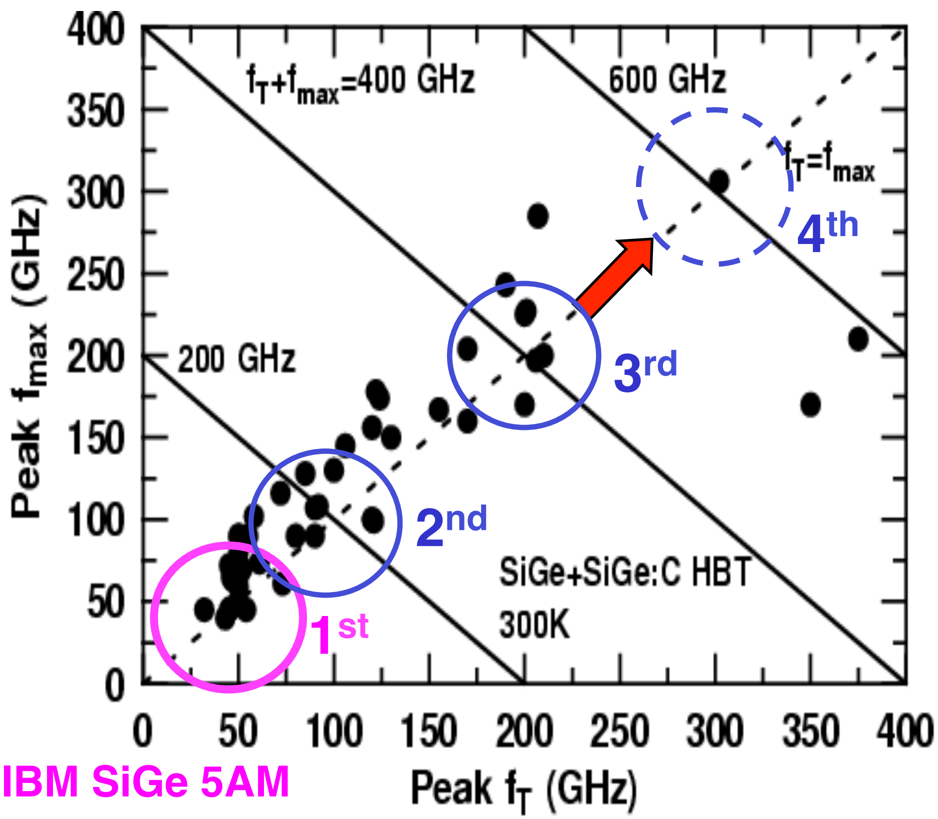
A World Class Team!

Part of the RHESE Program
M. Watson, PM
NASA-MSFC

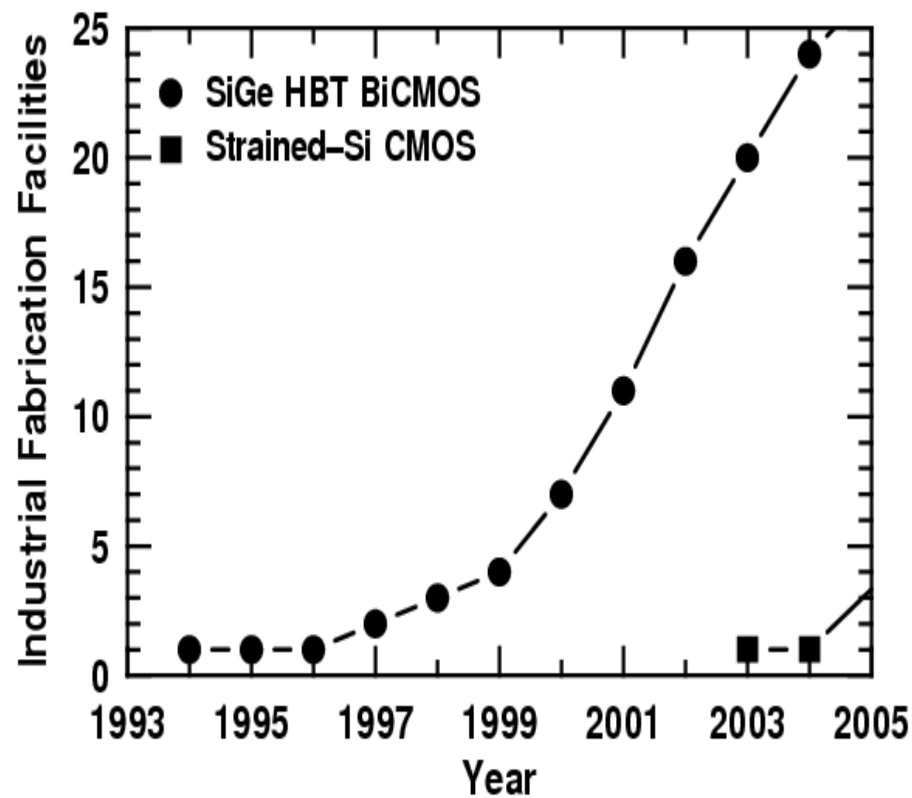
- **Georgia Tech**
  - John Cressler *et al.* (PI, devices, circuits)
  - Cliff Eckert (program management, reporting)
- **Auburn University**
  - Wayne Johnson *et al.* (packaging); Foster Dai *et al.* (circuit design); Guofu Niu *et al.* (profile design)
- **University of Tennessee**
  - Ben Blalock *et al.* (circuit design)
- **University of Maryland**
  - Patrick McCluskey *et al.* (reliability, physics of failure modeling)
- **Vanderbilt University**
  - Mike Alles, Robert Reed, *et al.* (radiation effects, TCAD)
- **JPL**
  - Mohammad Mojarradi *et al.* (applications, reliability testing, circuit design)
- **Boeing**
  - Leora Peltz *et al.* (applications, circuit design)
- **Lynguent / University of Arkansas**
  - Alan Mantooth *et al.* (modeling, circuits)
- **BAE Systems**
  - Ray Garbos, Rich Berger *et al.* (maturation, applications)
- **IBM**
  - Alvin Joseph *et al.* (SiGe technology fabrication)

The SiGe Success Story

- Rapid Generational Evolution (full SiGe BiCMOS)
- Significant In-roads in High-speed Communications ICs
- 100% Silicon Foundry Manufacturing Compatibility (low cost)



IBM SiGe 5AM

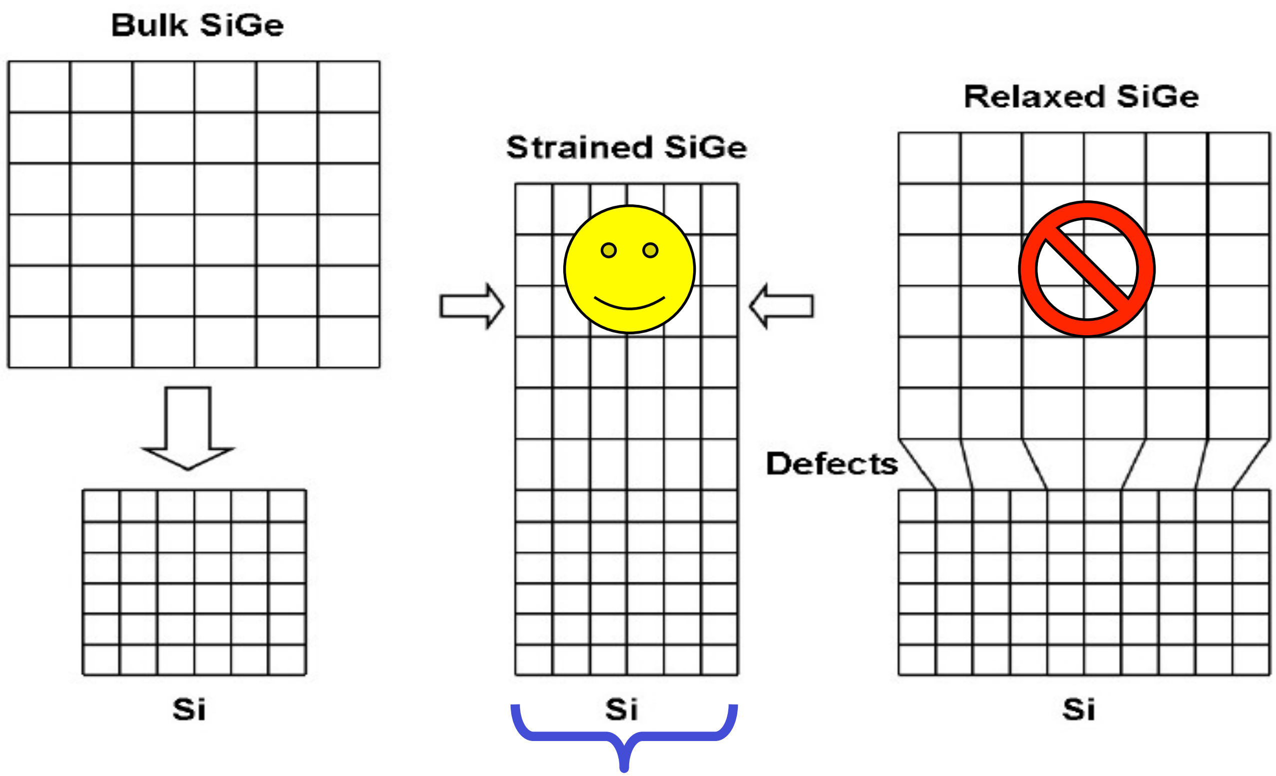


SiGe Strained Layer Epitaxy

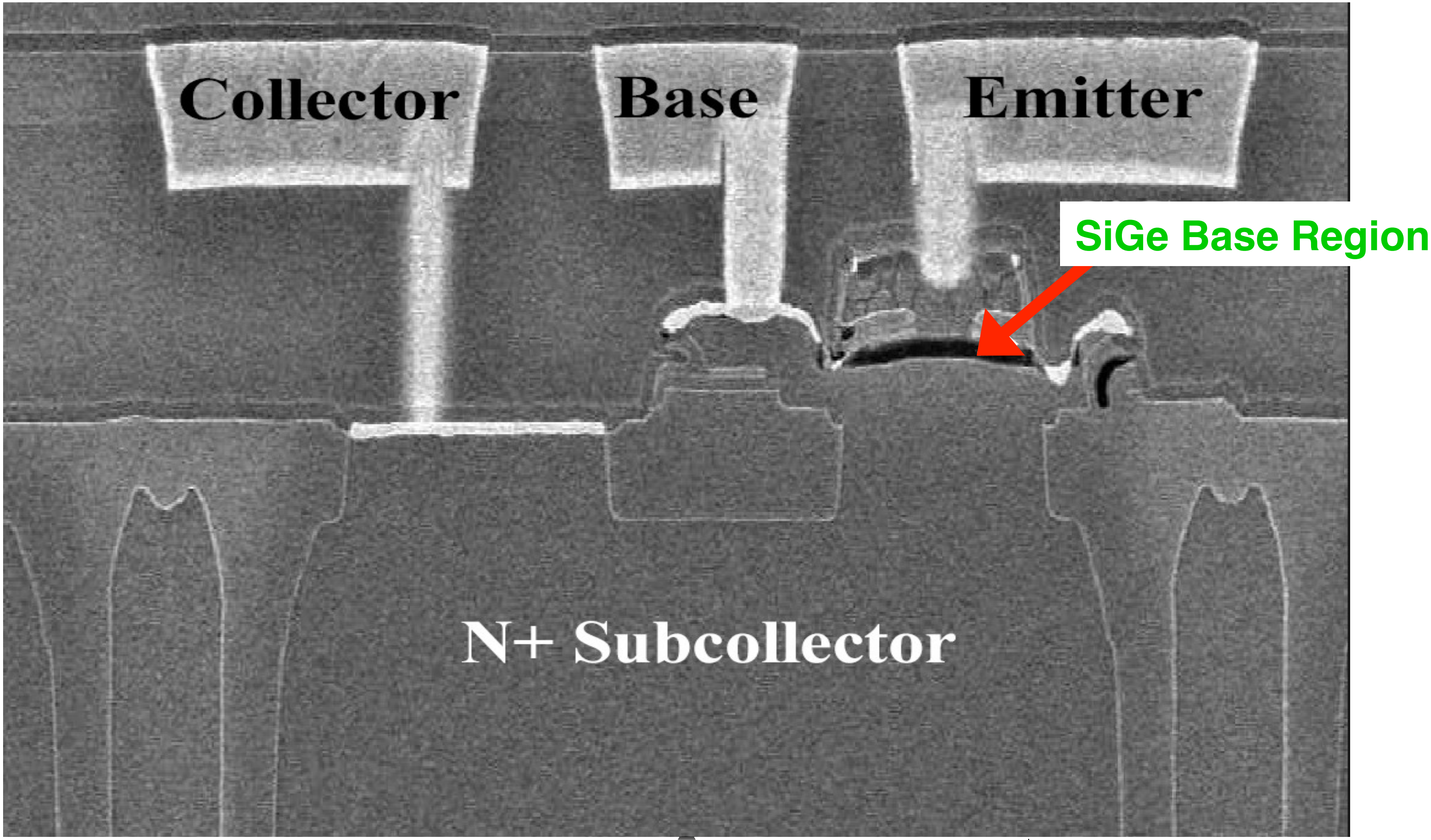
The Idea: Practice Bandgap Engineering (i.e., nanotechnology) in the Silicon Material System!

Introduce a small amount of Ge (smaller bandgap) into a Si BJT to …

Selectively tailor the transistor for improved performance!



A SiGe Transistor

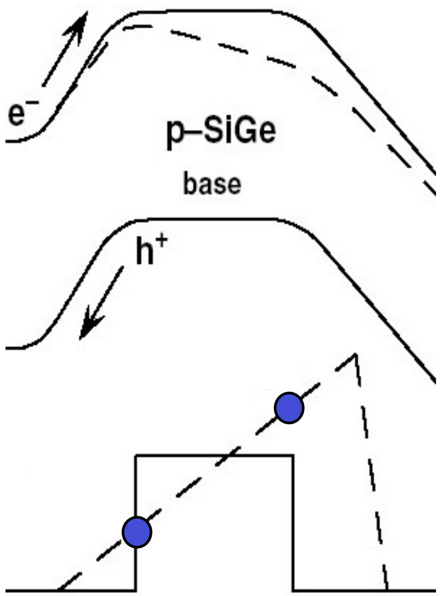


SiGe HBTs for Cryo-T

The Idea: Put Graded Ge Layer into the Base of a Si BJT

Primary Consequences:

- smaller base bandgap increases electron injection (β↑)
- field from graded base bandgap decreases base transit time (f_T↑)
- base bandgap grading produces higher Early voltage (V_A↑)



$$\left.\frac{\beta_{SiGe}}{\beta_{Si}}\right|_{V_{BE}} \equiv \Xi = \left\{ \frac{\tilde{\gamma}\,\tilde{\eta}\,\Delta E_{g,Ge}(grade)/kT \; e^{\Delta E_{g,Ge}(0)/kT}}{1 - e^{-\Delta E_{g,Ge}(grade)/kT}} \right\}$$

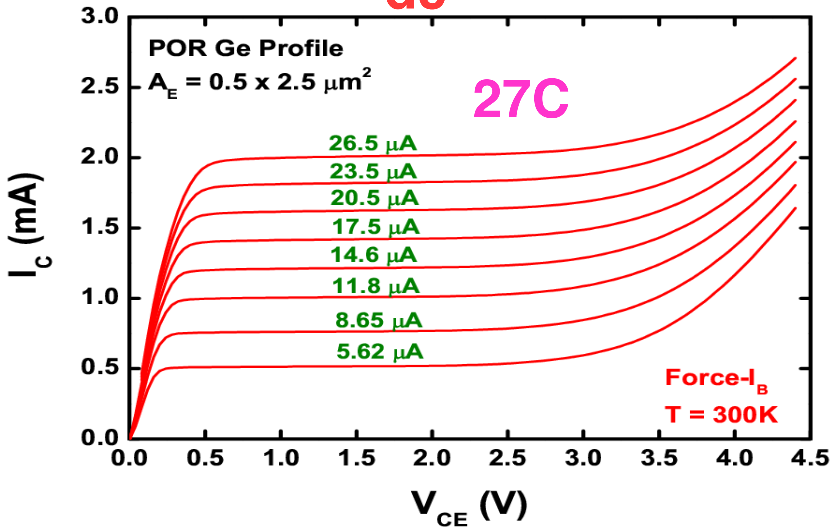
$$\frac{\tau_{b,SiGe}}{\tau_{b,Si}} = \frac{2}{\tilde{\eta}}\,\frac{kT}{\Delta E_{g,Ge}(grade)} \left\{ 1 - \frac{kT}{\Delta E_{g,Ge}(grade)} \left[1 - e^{-\Delta E_{g,Ge}(grade)/kT} \right] \right\}$$

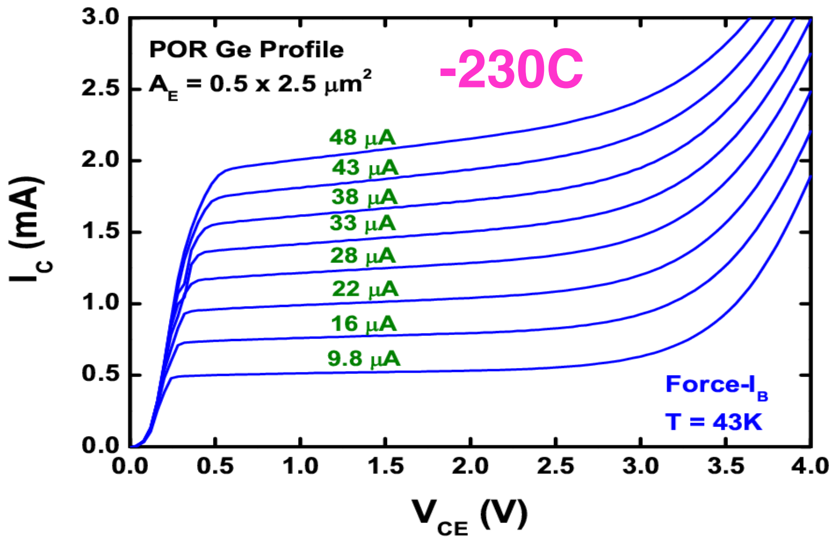
$$\left.\frac{V_{A,SiGe}}{V_{A,Si}}\right|_{V_{BE}} \equiv \Theta \simeq e^{\Delta E_{g,Ge}(grade)/kT} \left[\frac{1 - e^{-\Delta E_{g,Ge}(grade)/kT}}{\Delta E_{g,Ge}(grade)/kT} \right]$$

All kT Factors Are Arranged to Help at Cryo-T!

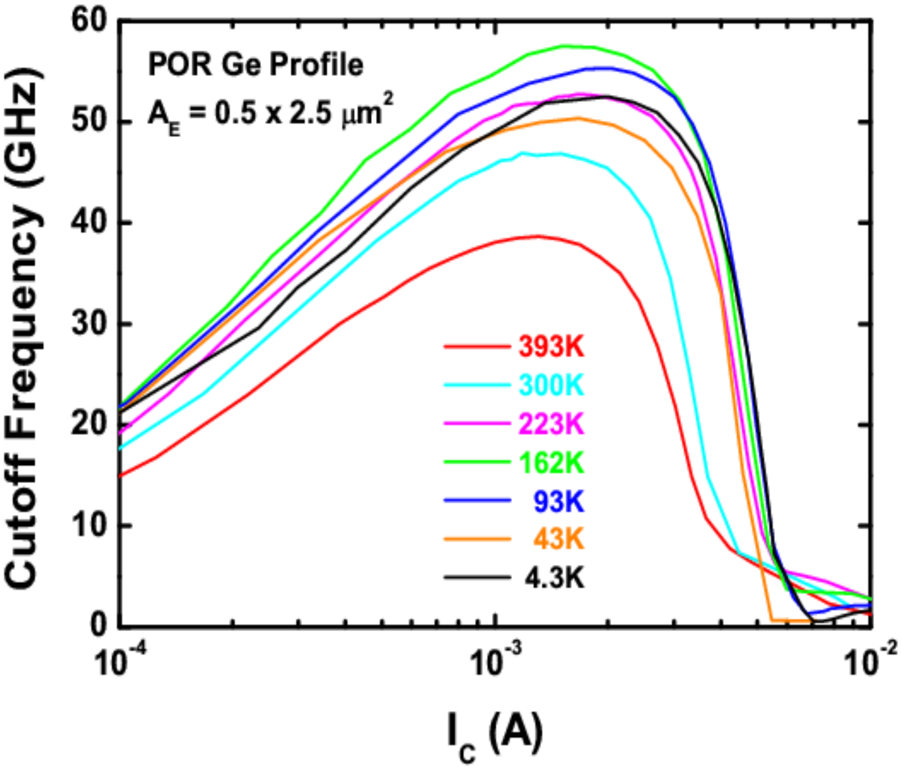
SiGe HBT Cryo-T Data (POR Ge Profile)

dc



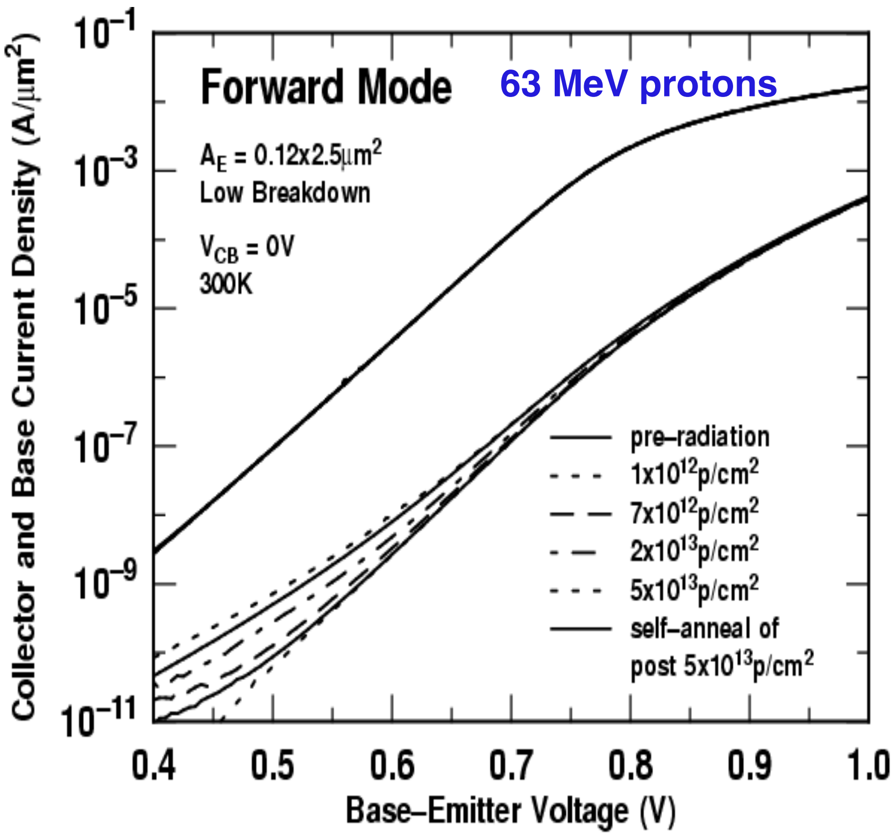


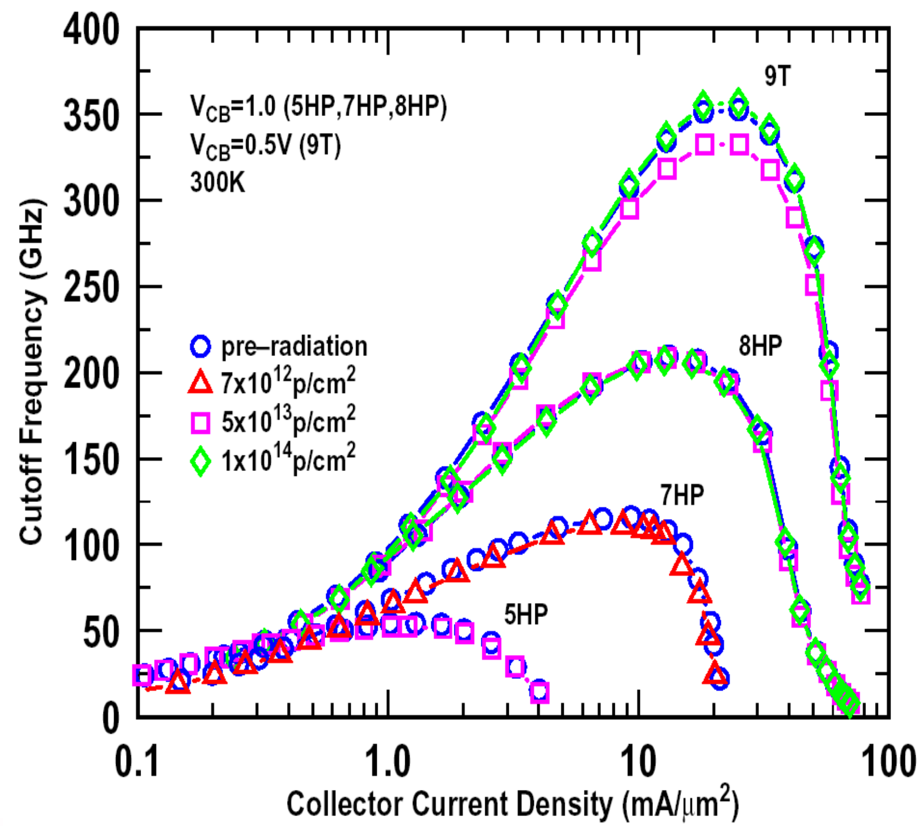
ac



Free Perk: Radiation Tolerance

- **Multi-Mrad Total Dose Hardness!** **(with no intentional hardening!)**
- **Radiation Hardness Due to Epitaxial Base Structure** **(not Ge)**
  - thin emitter-base spacer + heavily doped extrinsic base + very thin base



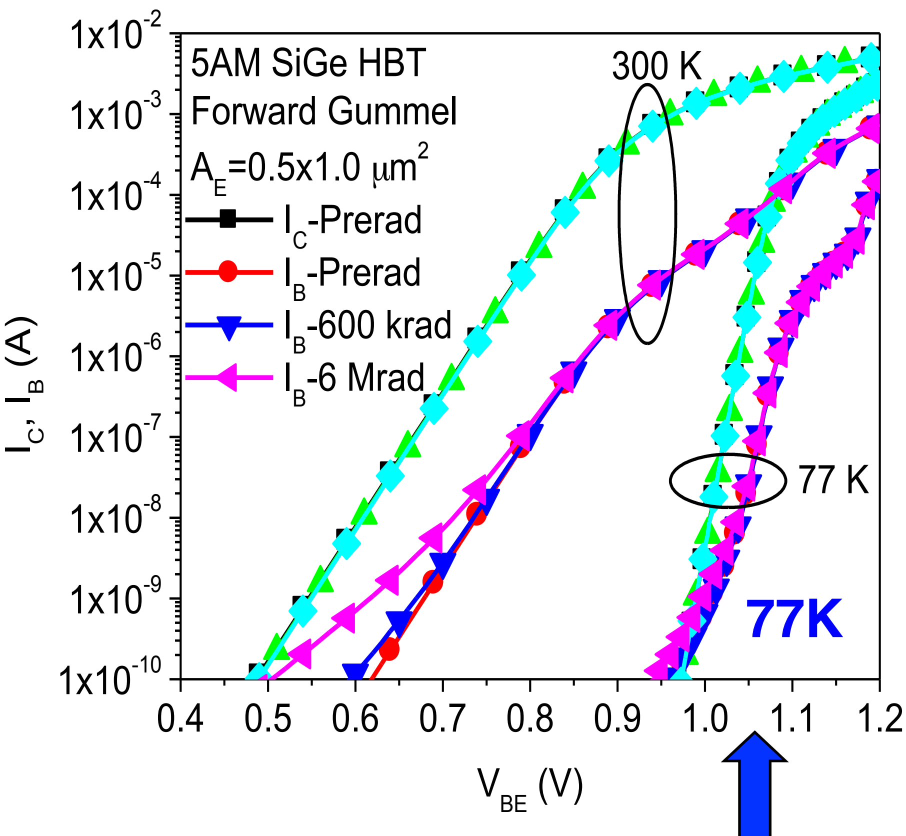


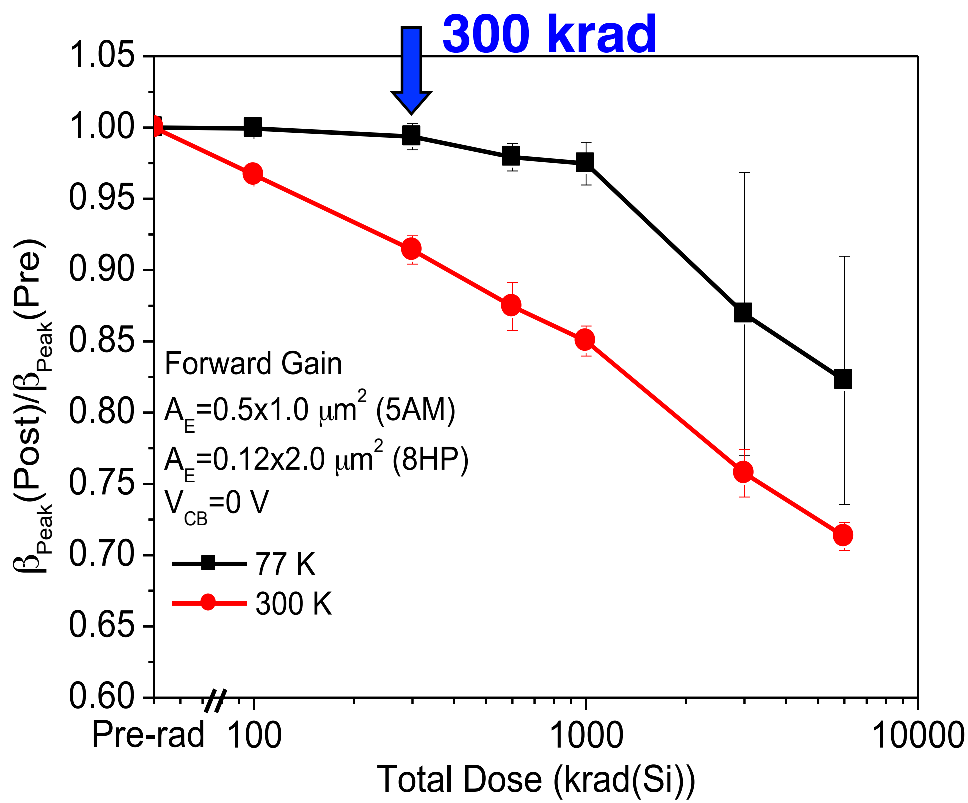
SiGe HBT Radiation Tolerance

First 77K Proton Irradiation Experiment in SiGe Technology

- 63 MeV protons at UC Davis (NASA-GSFC / DTRA collaboration)

- **Radiation Damage Smaller at 77K Than at 300K (great news!)**



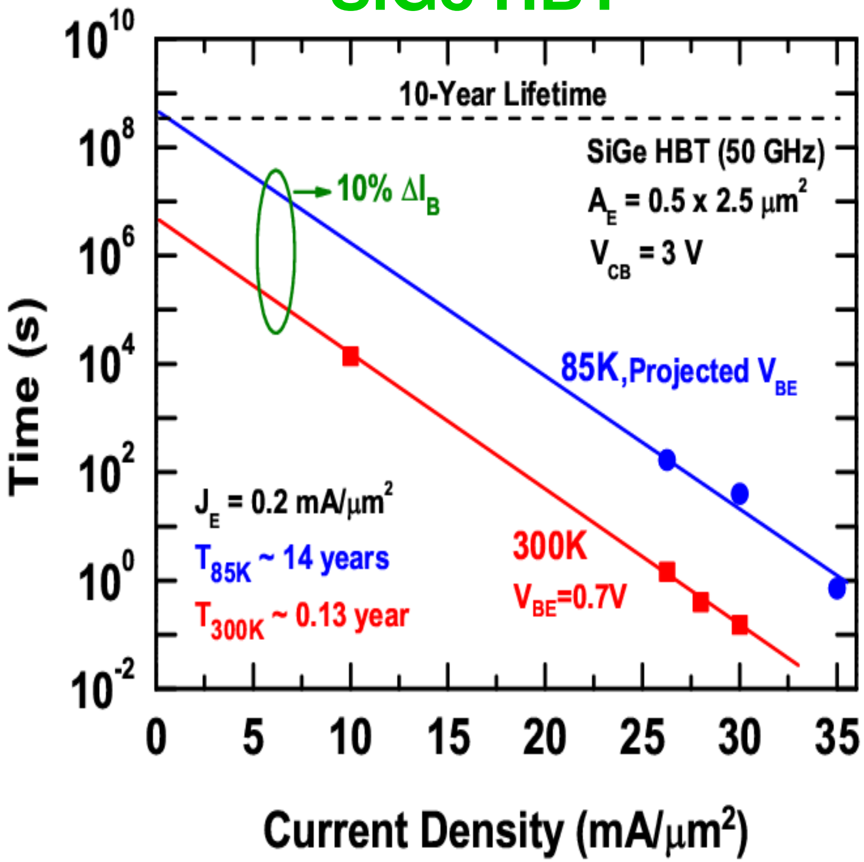


no change in peak β at 300 krad at 77K!

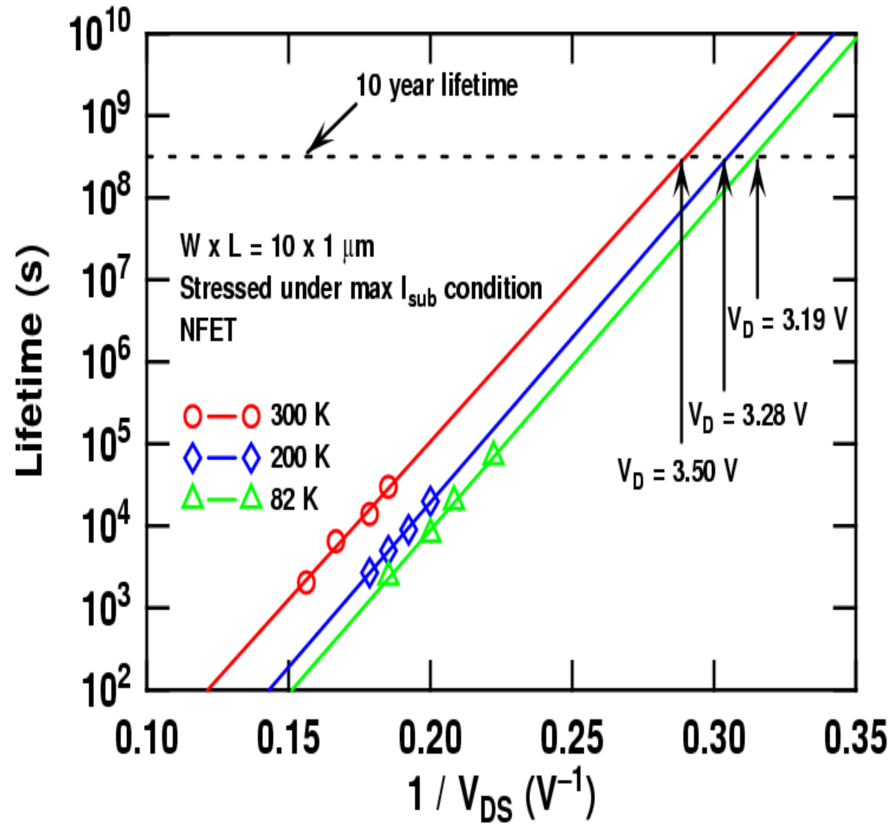
Device Reliability

- **Transistor Reliability Appears to be Fine at Cryo-T**

SiGe HBT



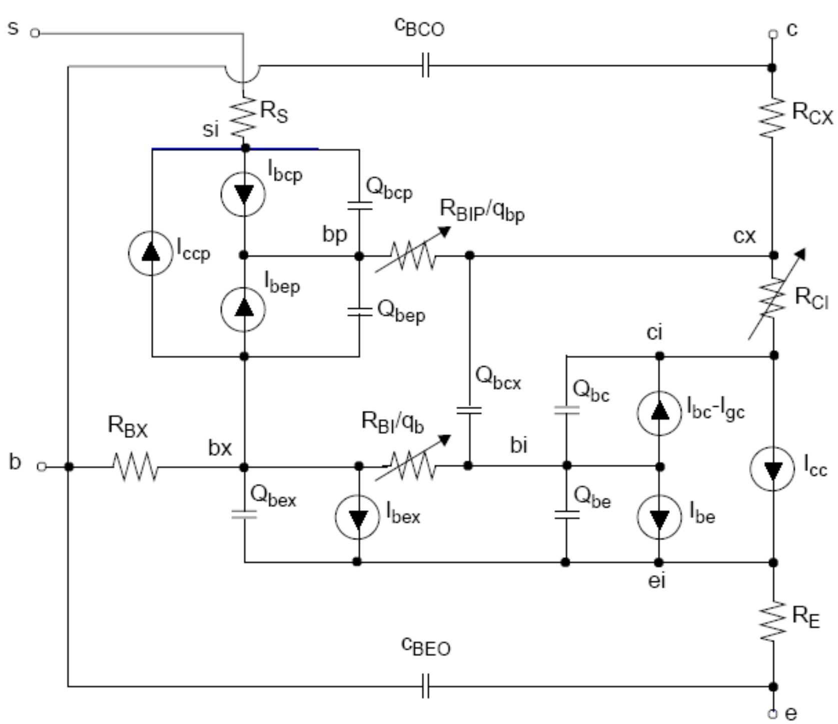
CMOS

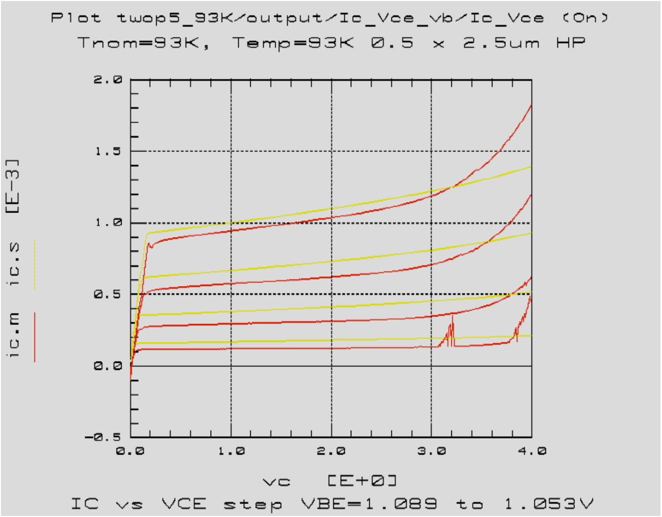


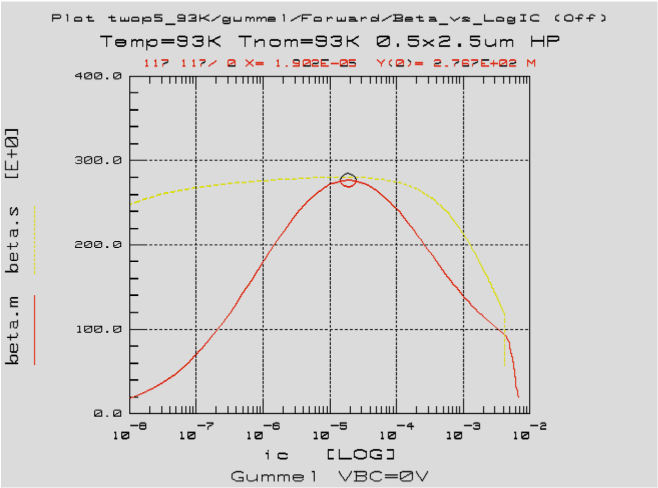
Compact Modeling Tools

-180 C

SiGe HBT VBIC Model







Remote Electronics Unit (REU)

REU Applications: Distributed Sensors, Processing, Control

Key Attributes: Flexible, Modular, Reconfigurable

Surface Operations
- Robotic Control – Distributed (LPRP)
- Control of science instrumentation or resources (LPRP)
- ISRU processing – sensing (LPRP) – sensors
- Long-term monitoring, low power (Mars Science)
- Infrastructure monitoring of power, communications (LPRP)

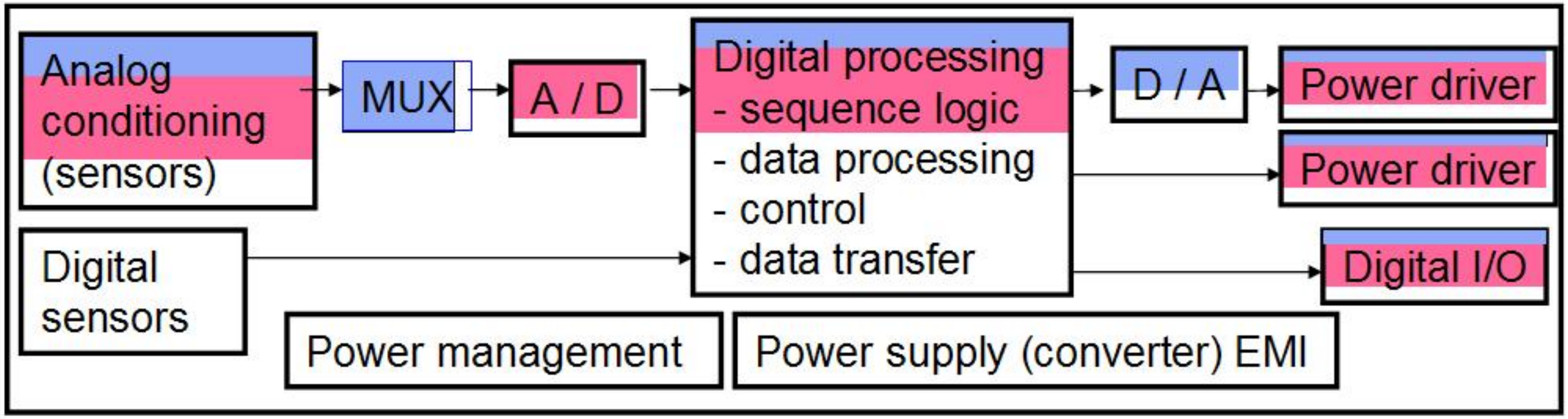
Spacecraft for Moon and Mars
- Large lander (LPRP, LSAM)
- CEV, CLV, CaLV, EDS
- Hopper (LPRP)
- Micro-spacecraft

Manned Missions
- Exterior climate monitoring
- Life support resources
- Facilities
- Robotic helpers

Timeline

Science Missions to Outer Planets
- Probe to Europa or Enceladus
- Titan aerobot
- Neptune atmospheric probe

SiGe REU Vision



Maintain Flexibility!

CRYO I – Did basic primitives needed for Analog conditioning, MUX, D/A, high voltage low current output driver, basic digital NAND, NOR gates, UART

CRYO II – Basic REU A/D (12 bits, 500kS/s), two analog conditioning strings using CRYO I building blocks, higher current - high voltage output driver, more complex digital circuits 16 registers, etc.), standard I/O, plus some additional primitives

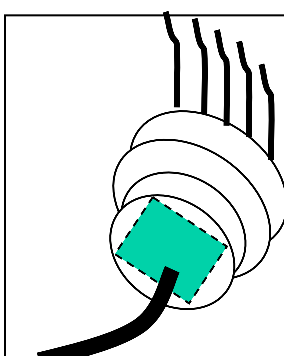
Sensor Types

Temperature
Strain
Pressure
Acceleration
Vibration
Acoustic
Heat Flux
Position
Rate
Flow

OLD – without output capability

32 channels
Standard Temp
100 in^3
5 #
25 Watts

NEW - in the connector housing



32 channels
Extreme Temp
1 in^3
0.5 #
0.5 Watts

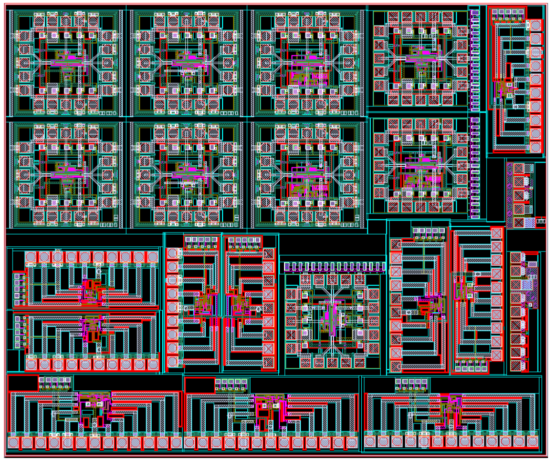
Phase I CRYO-I Target Circuits

(V_{DD} = 3.3V; Temperature = -180C to +120C)

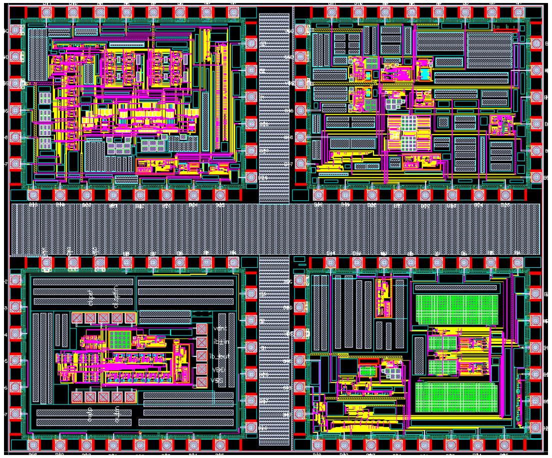
• General Purpose High-Z Input Operational Amplifier	UT
• Continuous-time Comparator	UT
• Precision Voltage References	UT, GT
• Sample and Hold Amplifiers	UT
• General Purpose Wideband Operational Amplifier	GT
• Precision Low-Drift Amplifier	UT
• Voltage Controlled Oscillator	AU
• Digital Library	AU
• Digital-to-Analog Converter (12 bit)	AU
• Power MOSFETs	JPL
• Driver for Power MOSFETs	JPL
• Under-Voltage Detector	JPL
• Analog Multiplexer	Lynguent
• Programmable Gain Amplifier	Lynguent
• Ramp Generator	Boeing

CRYO-I SiGe Circuit Designs

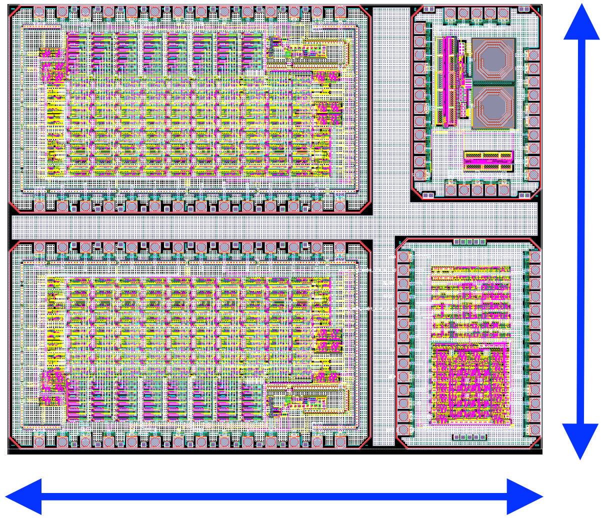
Georgia Tech



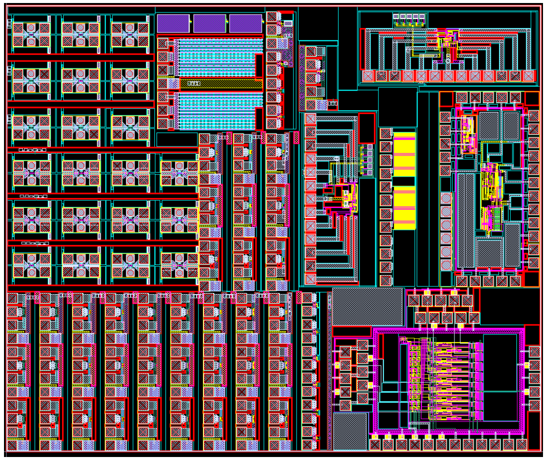
Tennessee



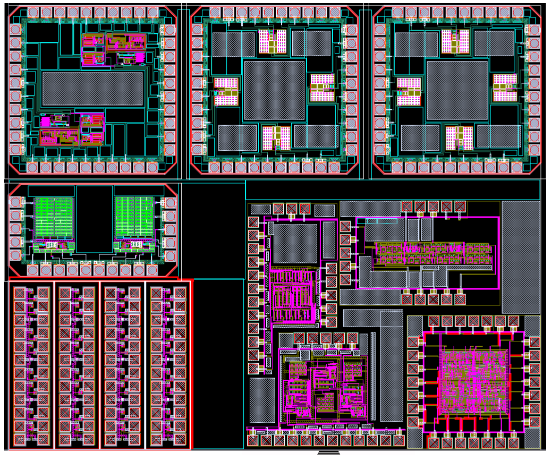
Auburn



GT / Arkansas



JPL / Boeing / Lynguent



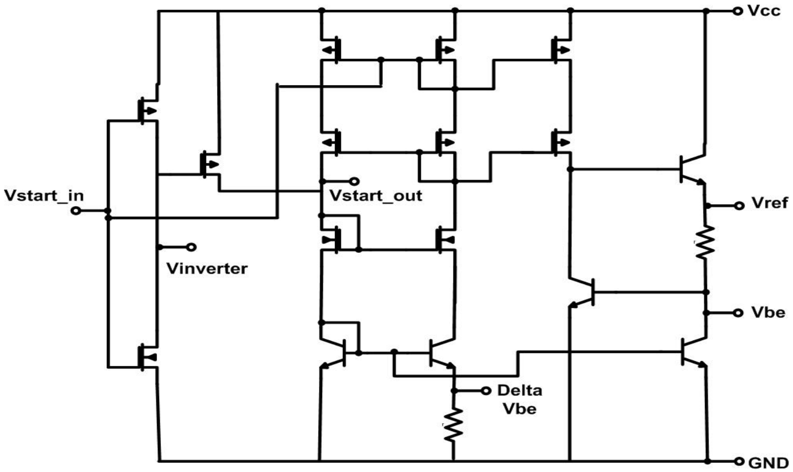
150 mm^2 of Real Estate!

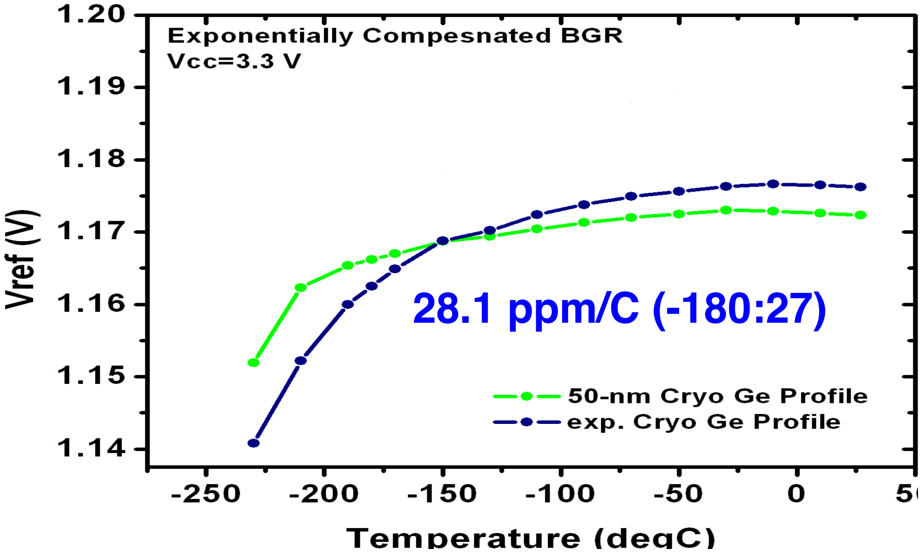
6 Design Teams!

Delivered On Schedule!

Voltage References

Comparison of Two Ge Profiles

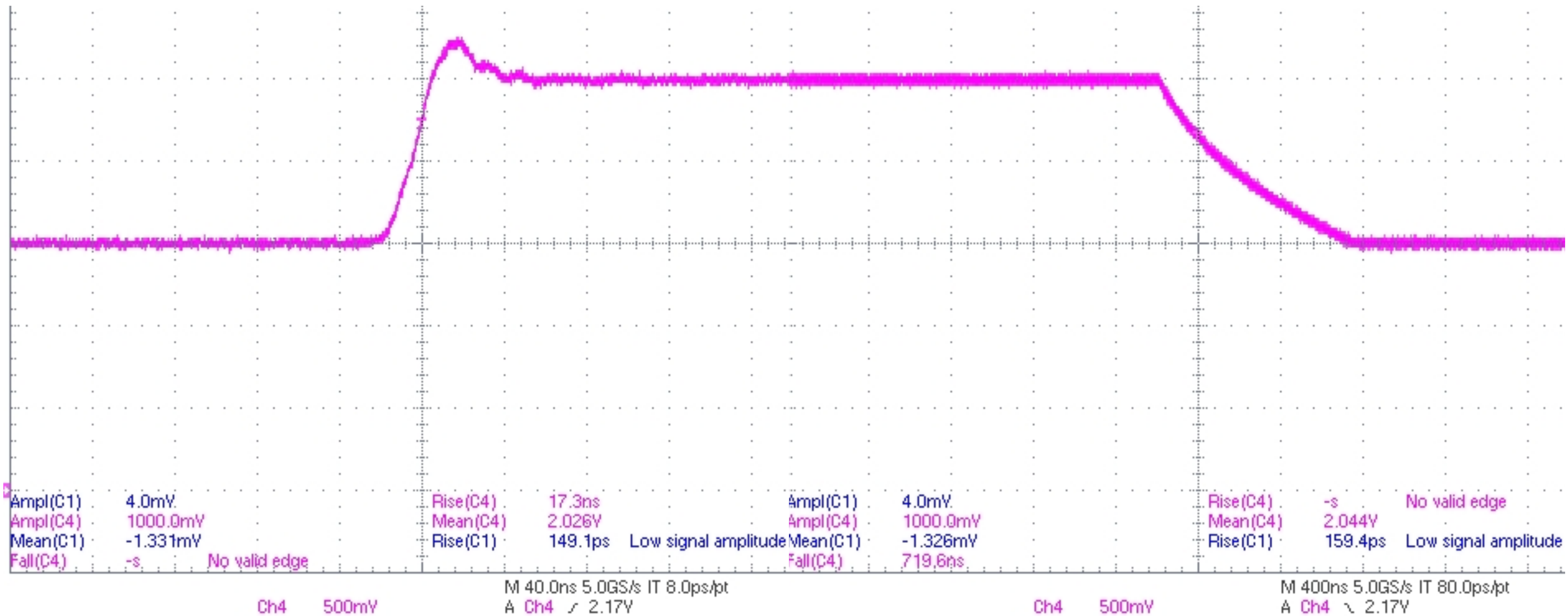




	exp. Ge Cryo	50 nm Ge Cryo
Vref @Vcc=3.3 V	1.176189 @ T= 27 degC	1.172259 @ T= 27 degC
	1.162533 @ T=-180 degC	1.166166 @ T=-180 degC
	1.140775 @ T=-230 degC	1.151884 @ T=-230 degC
TC(ppm/deg C) @ Vcc=3.3 V	10.6 over (-50: 27) degC	7.8 over (-50: 27) degC
	57.6 over (-180: 27) degC	28.1 over (-180: 27) degC
	118.4 over (-230: 27) degC	69.9 over (-230: 27) degC
Line Regulation over (2.5 V-4.3 V)	0.24% @ T=27 degC	0.43% @ T=27 degC
	0.30% @ T=-180 degC	0.93% @ T=-180 degC
	0.25% @ T=27 degC	0.90% @ T=27 degC

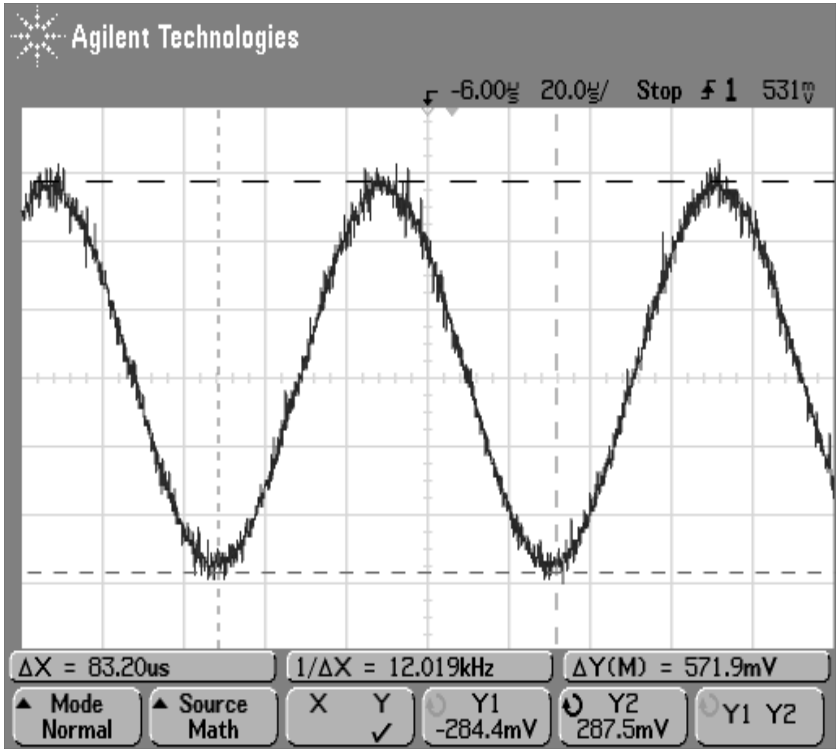
World's First 4.3K SiGe Op Amp!

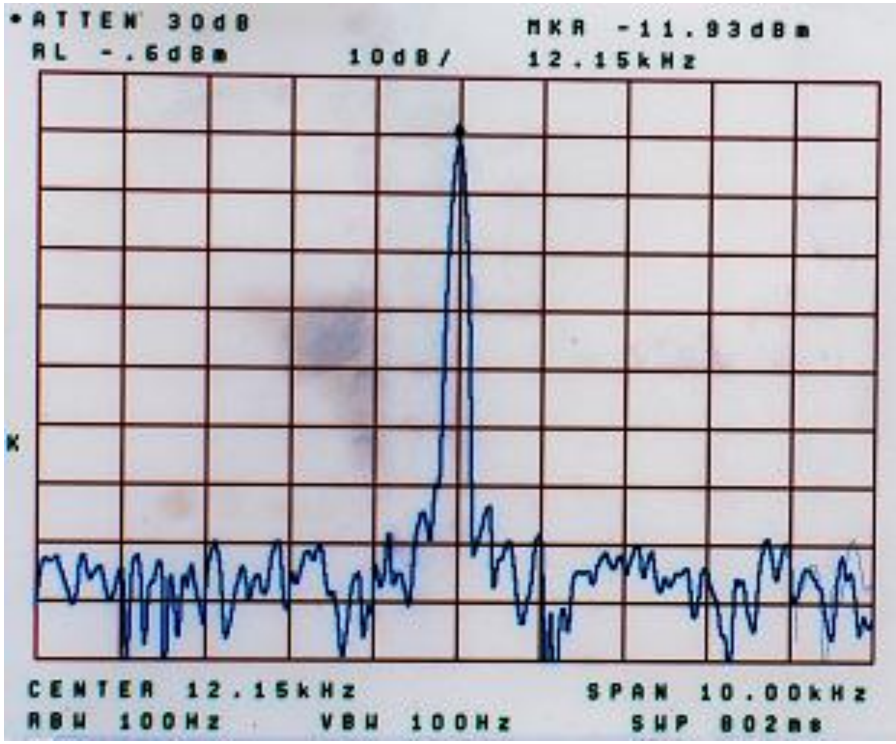
• **Output Slewing at 4.3K** (POR Ge)



12-bit DAC Functioning at -180C

Temp=-180C, f_{clk}=3.1MHz, OSR=128, f_{sig}=12KHz, no deglitch filter



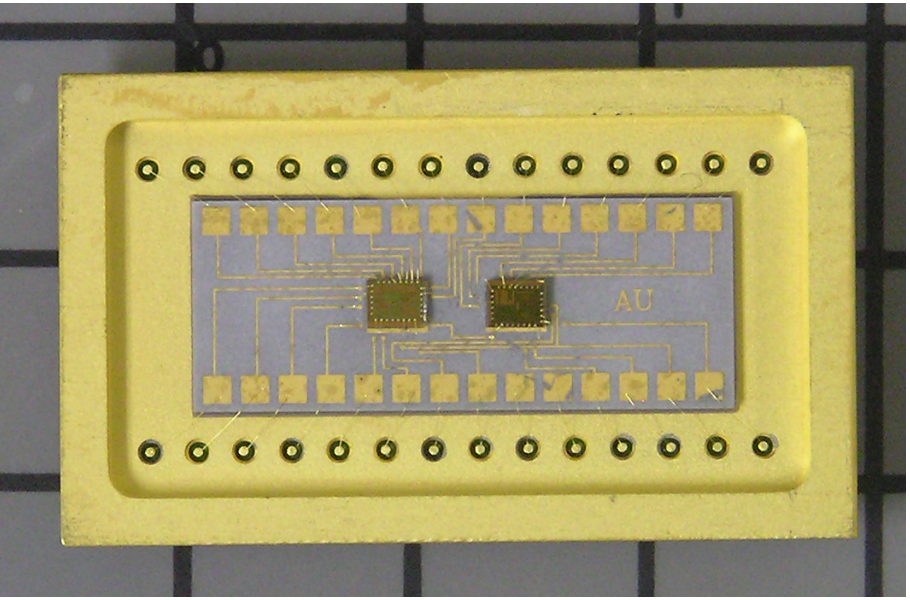


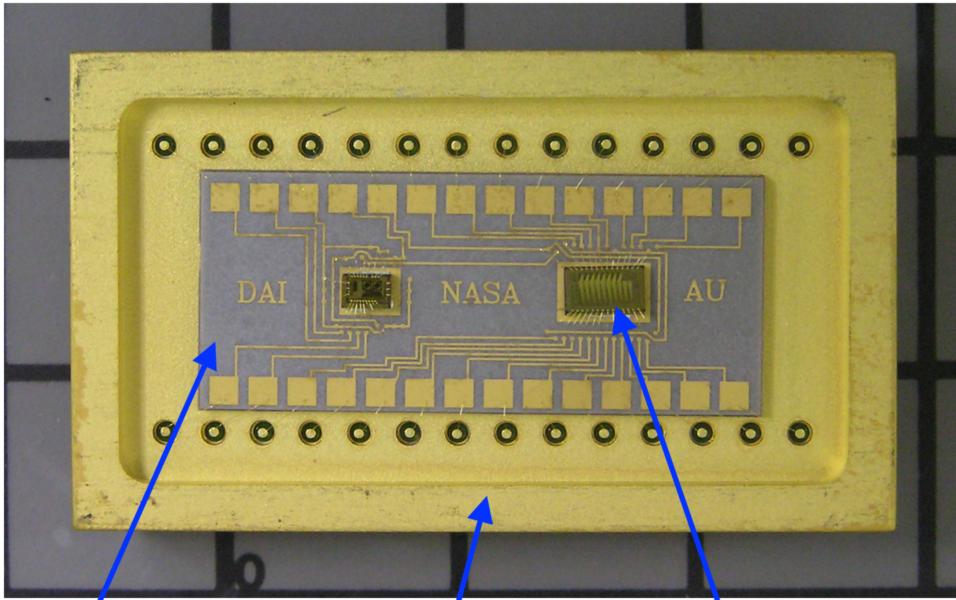
Single-ended output

Phase IIA Circuit Targets (Draft)

- **Low-power, Multi-channel Instrumentation ADC**
  - highly-integrated, power efficient, high sensor count SoCs for data acquisition
  - < 15 mW total power, 12-bit resolution, and 40 kS/s per channel
- **High-speed ADC for Specialized Sensors**
  - 10-bit resolution, 500-kS/s conversion rate
- **Prototype Analog Section of an REU Channel**
  - system demonstration using Phase I CRYO-I circuits
- **High-side and Low-side Gate Drivers (24 V)**
  - refined high voltage transistors
  - motor/actuator control and smart-power systems
- **Voltage Regulators**
- **Bus Interface**
- **Temperature Sensors**
- **Refine Selected Phase I Circuits**
  - emphasis on low power without sacrificing wide temperature capability
  - various op amps, voltage and current references, comparators, etc.

SiGe System-in-a-Package!





Si_3N_4 Substrate

AlSi Alloy

SiGe Die

Major Phase IIA Themes

- **Continue To Develop SiGe Technology For Lunar Applications**

- **Prove Reliability Over Temperature** (Devices + Circuits)
- **Define Step-2 Circuit Building Blocks** (Evolving Library)
- **Build an REU Path as a System-in-a-Package Prototype**
- **Refine Compact Modeling Tools** (Modeling Suite)
- **Finalize Robust Multi-chip Packaging Platform**
- **Refine Tools Packaging Reliability, Failure Modeling**
- **Establish Radiation Tolerance** (Devices + Circuits)
- **Perform Cycling / Soak Studies of Packaged Circuits**
- **Pursue Flight Opportunities / Flight Qualification Path(s)**

Summary

- **SiGe HBT BiCMOS Technology**
  - lots of progress – many new apps **(extreme environments / space)**
  - record speed of 510 GHz at 4.5K (lots of steam left!)
- **SiGe For Cryogenic Environments (and wide T swings!)**
  - major performance metrics improve with cooling (operation to 4K)
  - scaling improves things further (> 250 GHz and < 0.5 dB NF at 85K)
- **SiGe For Radiation Environments**
  - built-in total-dose hardness (multi-Mrad as fabricated!)
  - proven SEU mitigation approaches available if needed
- **Large NASA Project Developing SiGe for Space Apps**
  - devices + models + circuits + packages + reliability, etc.

SiGe Is Very Promising for Extreme Environments!